INTEGRATED CIRCUITS

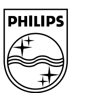
DATA SHEET

TDA3504
Video control combination circuit

Product specification
Supersedes data of April 1995
File under Integrated Circuits, IC02

1996 Jan 09

Philips Semiconductors




FEATURES

- Capacitive coupling of the colour difference and luminance input signals with black level clamping in the input stages
- Linear saturation control acting on the colour difference signals
- (G–Y) and RGB matrix
- Linear transmission of inserted signals
- Equal black levels for inserted and matrixed signals
- 3 identical channels for the RGB signals
- Linear contrast and brightness controls, operating on both the inserted and matrixed RGB signals
- Clamping, horizontal and vertical blanking of the three input signals controlled by a 3-level sandcastle pulse
- Emitter-follower outputs for driving the RGB output stages.

GENERAL DESCRIPTION

The TDA3504 is an integrated circuit which performs video control functions in a PAL/SECAM decoder for negative colour difference signals –(R–Y) and –(B–Y).

The required input signals are luminance and colour difference and a 3-level sandcastle pulse for control purposes. Linear RGB signals can be inserted from an external source. RGB output signals are available for driving the video output stages.

QUICK REFERENCE DATA

All voltages referenced to pin 18 (ground).

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 2)	–	12.0	–	V
I_P	supply current (pin 2)	–	95	–	mA
$V_{11(p-p)}$	video blanking sync (VBS) input signal (peak-to-peak value)	–	0.45	–	V
$V_{15(p-p)}$	–(B–Y) colour difference input signal (peak-to-peak value)	–	1.33	–	V
$V_{14(p-p)}$	–(R–Y) colour difference input signal (peak-to-peak value)	–	1.05	–	V
$V_{10, 9, 8(b-w)}$	inserted RGB signals (black-to-white value)	–	1.0	–	V
V_6	3-level sandcastle pulse				
	level 1	–	2.5	–	V
	level 2	–	4.5	–	V
	level 3	–	8.0	–	V
V_{17}	control voltage brightness	1.0	–	3.0	V
V_{16}	control voltage contrast	2.0	–	4.2	V
V_{12}	control voltage saturation	2.0	–	4.2	V
T_{amb}	operating ambient temperature	0	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3504	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1

BLOCK DIAGRAM

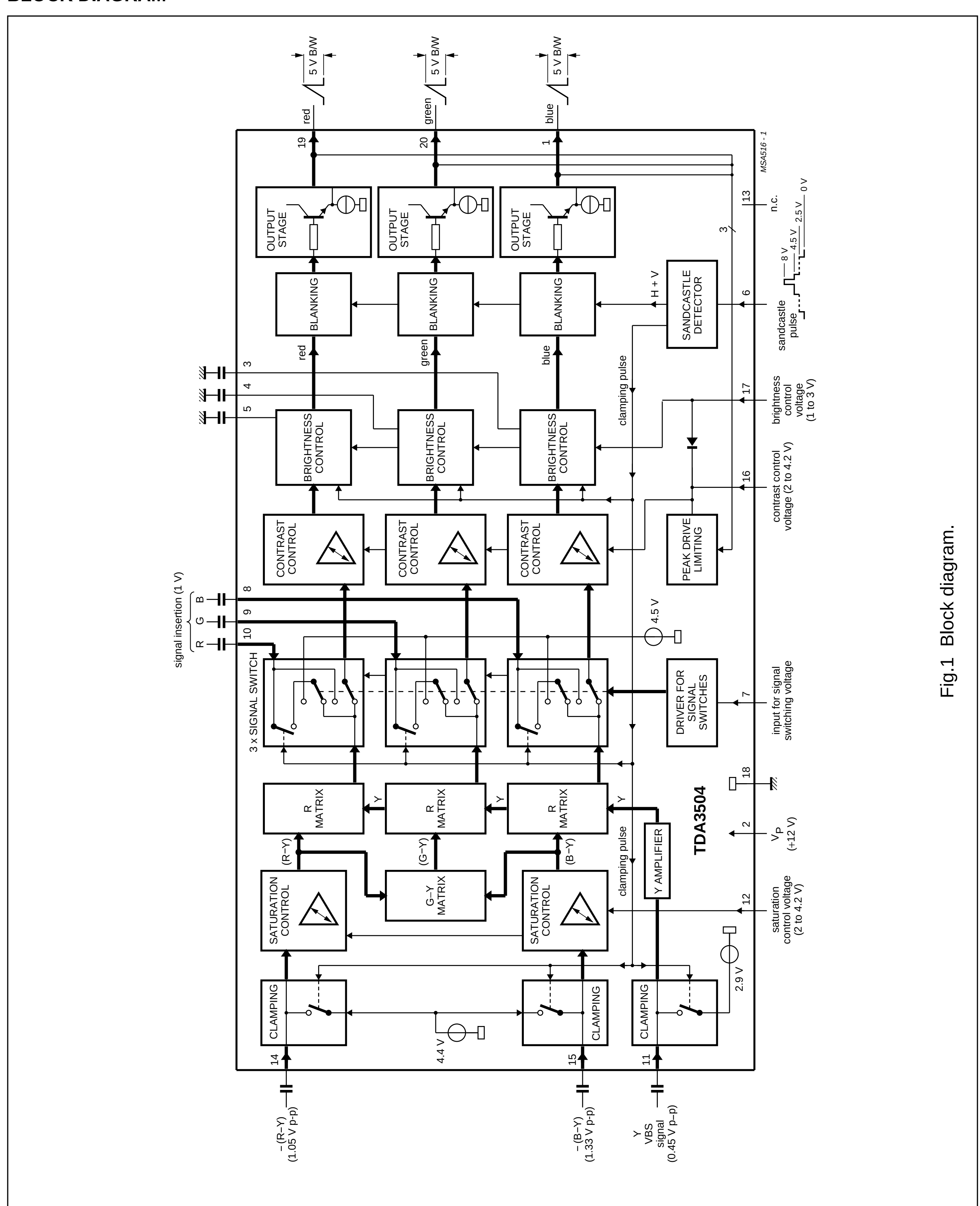


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
BO	1	blue output
V_P	2	supply voltage (+12 V)
CB	3	blue storage capacitor for brightness
CG	4	green storage capacitor for brightness
CR	5	red storage capacitor for brightness
SAND	6	sandcastle pulse input
FSW	7	fast switch for RGB input
BI	8	blue input (external signal)
GI	9	green input (external signal)
RI	10	red input (external signal)
Y	11	luminance input
SAT	12	saturation control input
n.c.	13	not connected
–(R–Y)	14	colour difference input
–(B–Y)	15	colour difference input
CON	16	contrast control input
BRI	17	brightness control input
GND	18	ground (0 V)
RO	19	red output
GO	20	green output

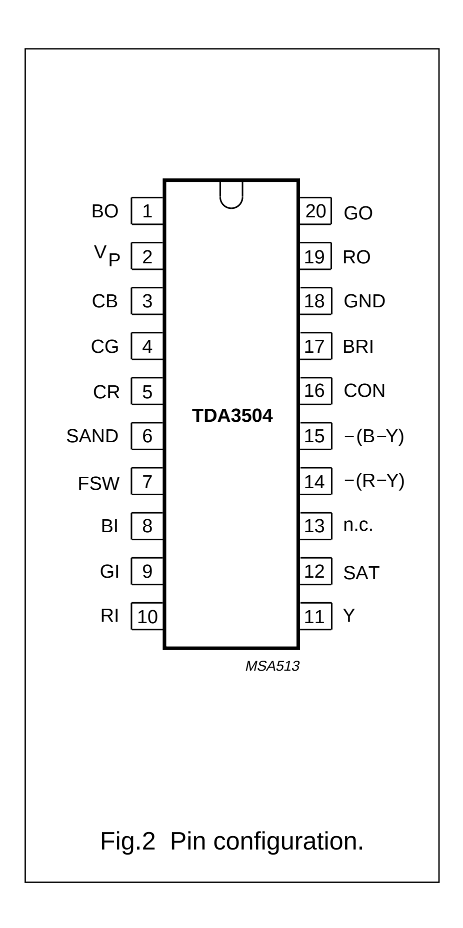


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 2)	0	13.2	V
V_6	sandcastle voltage (pin 6)	0	V_P	V
V_7	fast switch voltage (pin 7)	–0.5	+3.0	V
$V_{12, 16, 17}$	control input voltage (pins 12, 16 and 17)	0	$0.5V_P$	V
V_n	voltage on pins 1, 3, 4, 5, 8 to 11, 14, 15, 19 and 20	no external DC voltage		
$I_{1, 19, 20 (av)}$	average output current (pins 1, 19 and 20)	–	–3	mA
$I_{1, 19, 20(max)}$	maximum output current (pins 1, 19 and 20)	–	–10	mA
$I_{16 (av)}$	average output current (pin 16)	–	10	mA
I_{17}	input current (pin 17)	–	5	mA
P_{tot}	total power dissipation	–	1.7	W
T_{amb}	operating ambient temperature	0	+70	°C
T_{stg}	storage temperature	–25	+150	°C

CHARACTERISTICS

V_P = 12 V; $V_{8,\,9,\,10(p\text{-}p)}$ = 1 V; $V_{11(p\text{-}p)}$ = 0.45 V; $V_{14(p\text{-}p)}$ = 1.05 V; $V_{15(p\text{-}p)}$ = 1.33 V; T_{amb} = 25 °C; measured in Figs 3 and 4; nominal settings of brightness (V_{17} = 2 V), contrast (V_{16} = 3.6 V) and saturation (V_{12} = 3.1 V); all voltages referenced to ground (pin 18); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage (pin 2)		10.8	12.0	13.2	V
I_P	supply current (pin 2)	note 1	65	95	125	mA
Colour difference inputs (pins 14 and 15)						
$V_{14(p\text{-}p)}$	–(R–Y) input signal (pin 14) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.05	1.48	V
$V_{15(p\text{-}p)}$	–(B–Y) input signal (pin 15) (peak-to-peak value)	for saturated colour bar with 75% of maximum amplitude	–	1.33	1.88	V
$\lvert I_{14,\,15}\rvert$	input current between clamping pulses		–	–	0.2	µA
$R_{14,\,15}$	input resistance		1.0	–	–	MΩ
$V_{14,\,15}$	internal DC voltage due to clamping	note 2	3.8	4.2	4.8	V
Saturation control (pin 12)						
V_{12}	control voltages(2)	maximum saturation	4.0	4.2	4.4	V
		nominal saturation 6 dB below maximum	2.9	3.1	3.3	V
		–26 dB saturation referenced to maximum	1.9	2.1	2.3	V
SAT	minimum saturation	V_{12} = 1.8 V	46	50	–	dB
I_I	input current		–	–	20	µA
(G–Y) matrix (see note 3)						
Luminance input (pin 11)						
$V_{11(p\text{-}p)}$	VBS input signal (peak-to-peak value)	note 4	–	450	630	mV
$\lvert I_{11}\rvert$	input current between clamping pulses		–	–	0.4	µA
R_{11}	input resistance		1.0	–	–	MΩ
V_{11}	input DC voltage due to clamping	note 2	2.5	2.9	3.3	V
m	linearity	nominal settings	0.85	–	–	
RGB channels						
SIGNAL SWITCHING INPUT (PIN 7)						
V_7	normal state voltage; no insertion		0	–	0.4	V
V_7	voltage level for insertion on		0.9	–	3.0	V
C_i	input capacitance		–	–	10	pF
I_I	input current	V_7 = 0 to 3 V	–100	–	+430	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SIGNAL INSERTION: RI (PIN 10); GI (PIN 9); BI (PIN 8)						
$V_{8, 9, 10(b-w)}$	external RGB input signals (black-to-white value)		–	1.0	1.4	V
$\lvert I_{8, 9, 10} \rvert$	input current between clamping pulses		–	–	0.5	μA
$V_{8, 9, 10}$	internal DC voltage due to clamping	notes 2 and 5	4.0	4.5	5.0	V
Contrast control (pin 16)						
V_{16}	control voltages(2)	maximum contrast	4.0	4.2	4.4	V
		nominal contrast 3 dB below maximum	3.4	3.6	3.8	V
		–10 dB below maximum	2.6	2.8	3.0	V
CON	minimum contrast	referenced to maximum; V_{16} = 2 V	17	21	29	dB
RGB_{diff}	difference between RGB channels	contrast –10 dB below maximum	–	–	0.6	dB
Peak drive limiting						
V_{th}	threshold voltage	note 2	8.5	8.8	9.1	V
I_{16}	input current at contrast control input	$V_{1, 19, 20} \geq V_{th}$	10	20	30	mA
	internal signal limiting	referenced to nominal output amplitude; note 6	110	–	–	%
Brightness control (pin 17)						
V_{17}	control voltages(2)	brightness control range	1.0	–	3.0	V
		nominal brightness	–	2.0	–	V
I_I	input current	no beam current limiting; V_{17} = 1 to 3 V	–	–	–10	μA
$\Delta V_{blk(b-w)}$	shift of black level in the control range referenced to the luminance signal (black-to-white value)	ΔV_{17} = 1 V	–	40	–	%
	tracking		95	–	–	%
RGB outputs (emitter follower; pins 19, 20 and 1)						
$V_{19, 20, 1}$	output voltage	black-to-white positive	4.0	5.0	6.5	V
$\Delta V_{19, 20, 1}$	difference in black level between RGB channels due to variation of contrast control		–	–	10	mV
$\lvert I_{19, 20, 1} \rvert$	internal current source		2.0	3.0	4.0	mA
Gain data (at nominal brightness, contrast, saturation and white point settings)						
$G_{v19, 20, 1-11}$	voltage gain with respect to luminance input (pin 11)		22	24	26	dB
$\alpha_{19, 20, 1-11}$	frequency response of luminance path	f = 0 to 5 MHz	–	–	3	dB

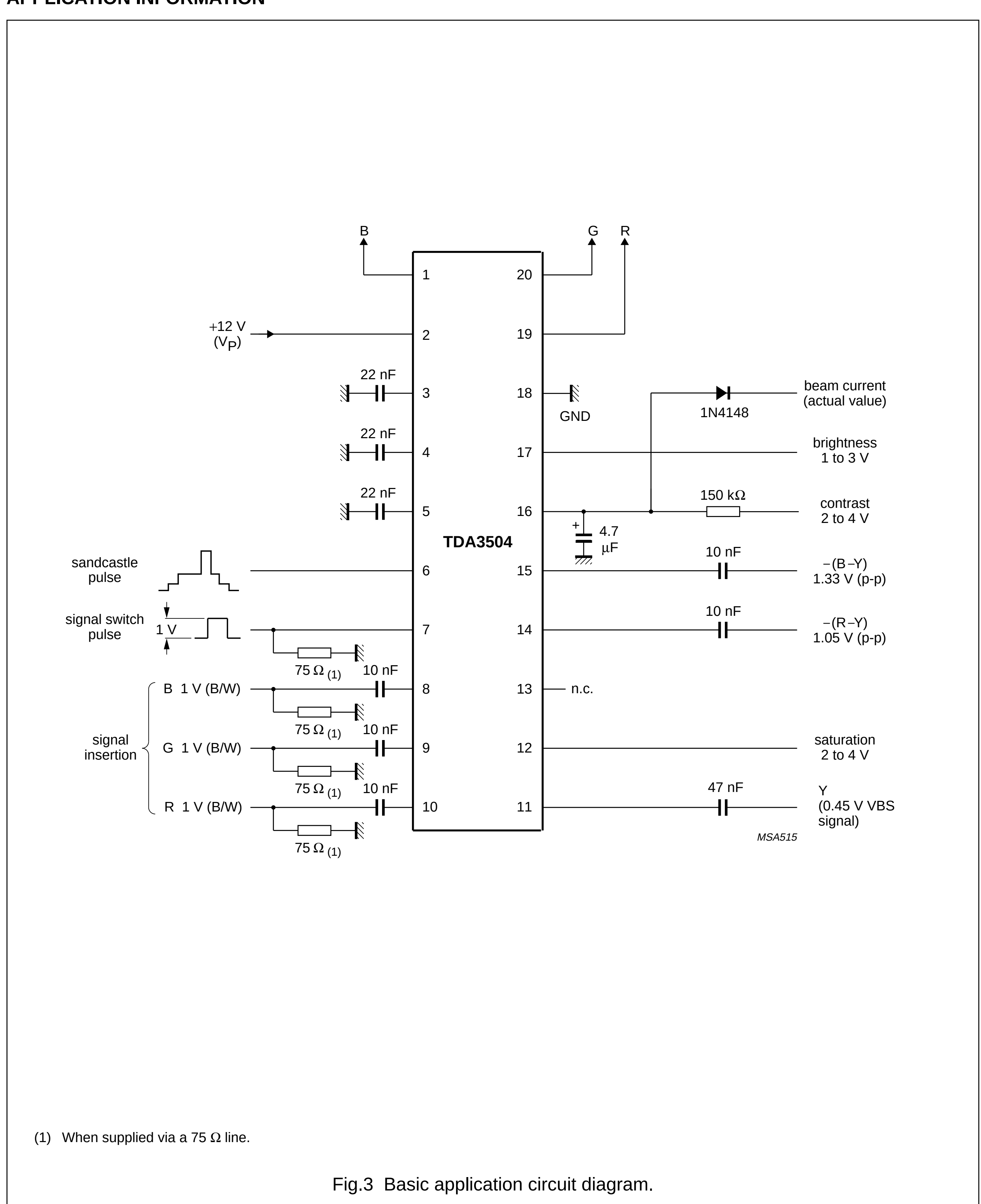
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_{v1-15}; G_{v19-14}	voltage gain with respect to colour difference inputs (pins 14 and 15)		11	14	17	dB
α_{1-15}; α_{19-14}	frequency response of colour difference paths	f = 0 to 2 MHz	–	–	3	dB
G_{v19-10}; G_{v20-9}; G_{v1-8}	voltage gain with respect to inserted signals		12	14	16	dB
α_{19-10}; α_{20-9}; α_{1-8}	frequency response of inserted signal paths	f = 0 to 10 MHz	–	–	3	dB
$\Delta t_{19, 20, 1}$	difference in transition times between R, G and B channels		–	0	15	ns
t_d	delay time between signal switching and signal insertion		–25	–	+25	ns
$\Delta G_{19, 20, 1}$	difference in gain between normal and signal insertion mode		–	–	10	%
Sandcastle pulse detector (pin 6)						
V_6	the following amplitudes are required for separating the various pulses	horizontal and vertical blanking; notes 7 and 8	2.1	2.5	2.9	V
		horizontal; note 7	4.1	4.5	5.0	V
		clamping; notes 7 and 9	7.6	8.0	12.0	V
		no keying; note 7	–	–	1.0	V
I_I	input current	LOW	–	–	–110	µA
t_d	delay of leading edge of clamping pulse		–	0.5	–	µs

Notes

1. Maximum value 110 mA after warm-up.
2. Values are proportional to the supply voltage.
3. Matrixed according to equation $V_{(G-Y)} = -0.51V_{-(R-Y)} - 0.19V_{-(B-Y)}$.
4. Clipping due to internal signal limitation may occur when the Y input is greater than nominal and maximum contrast and minimum brightness.
5. When V_{7-18} < 0.4 V during clamping time, the black levels of the inserted RGB signals are clamped on the black levels of the internal RGB signals.

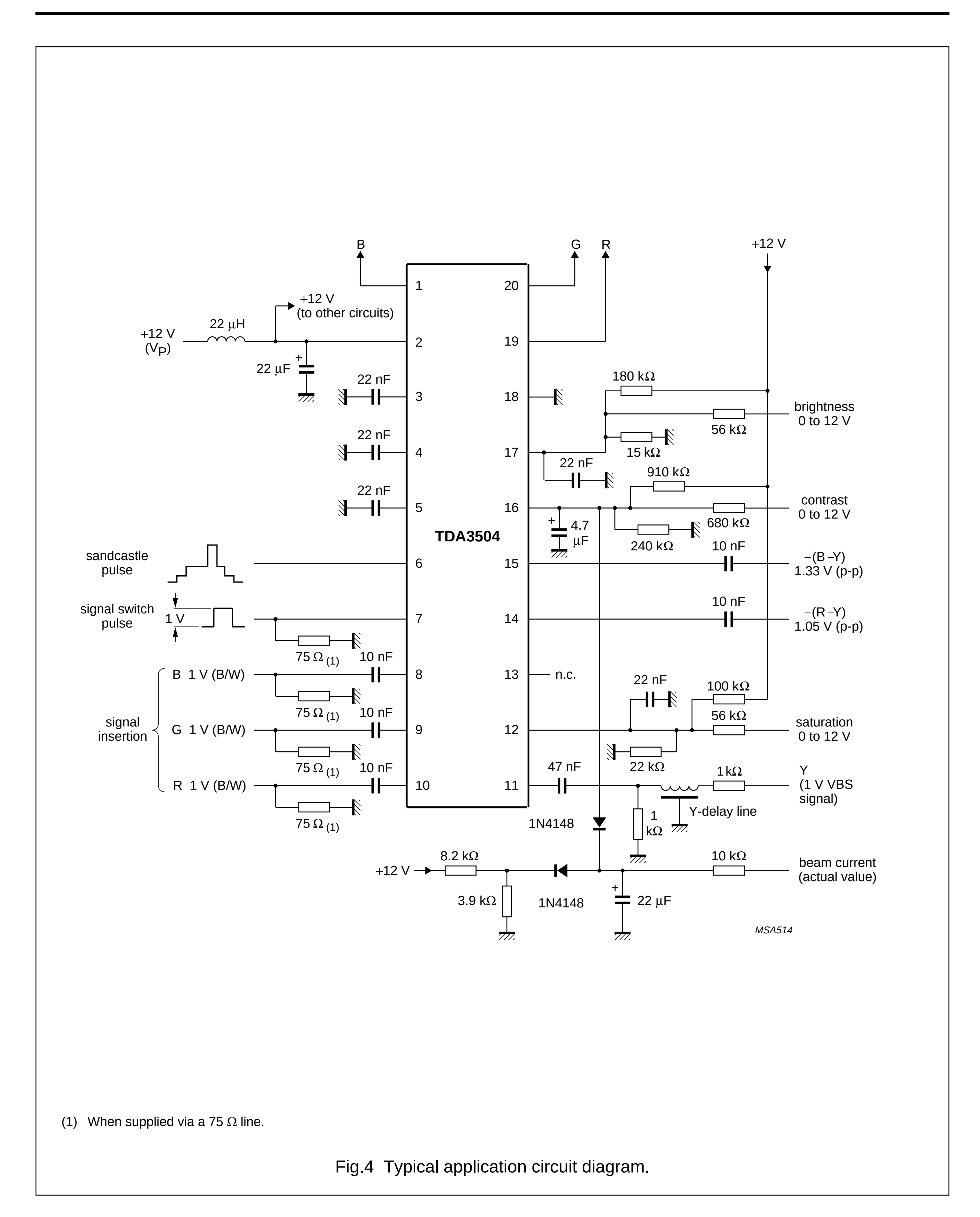
   When V_{7-18} > 0.9 V during clamping time, the black levels of the inserted RGB signals are clamped on an internal DC voltage (correct clamping of the external RGB signals is possible only when they are synchronous with the sandcastle pulse).
6. Internal signal limitation is allowed to start at 5.5 V after warm-up time.
7. The sandcastle pulse is compared with three internal thresholds (proportional to V_P) and the given levels separate the various pulses.
8. Blanked to ultra-black (–25%).
9. Pulse duration ≥3.5 µs.

APPLICATION INFORMATION



(1) When supplied via a 75 Ω line.

Fig.3 Basic application circuit diagram.

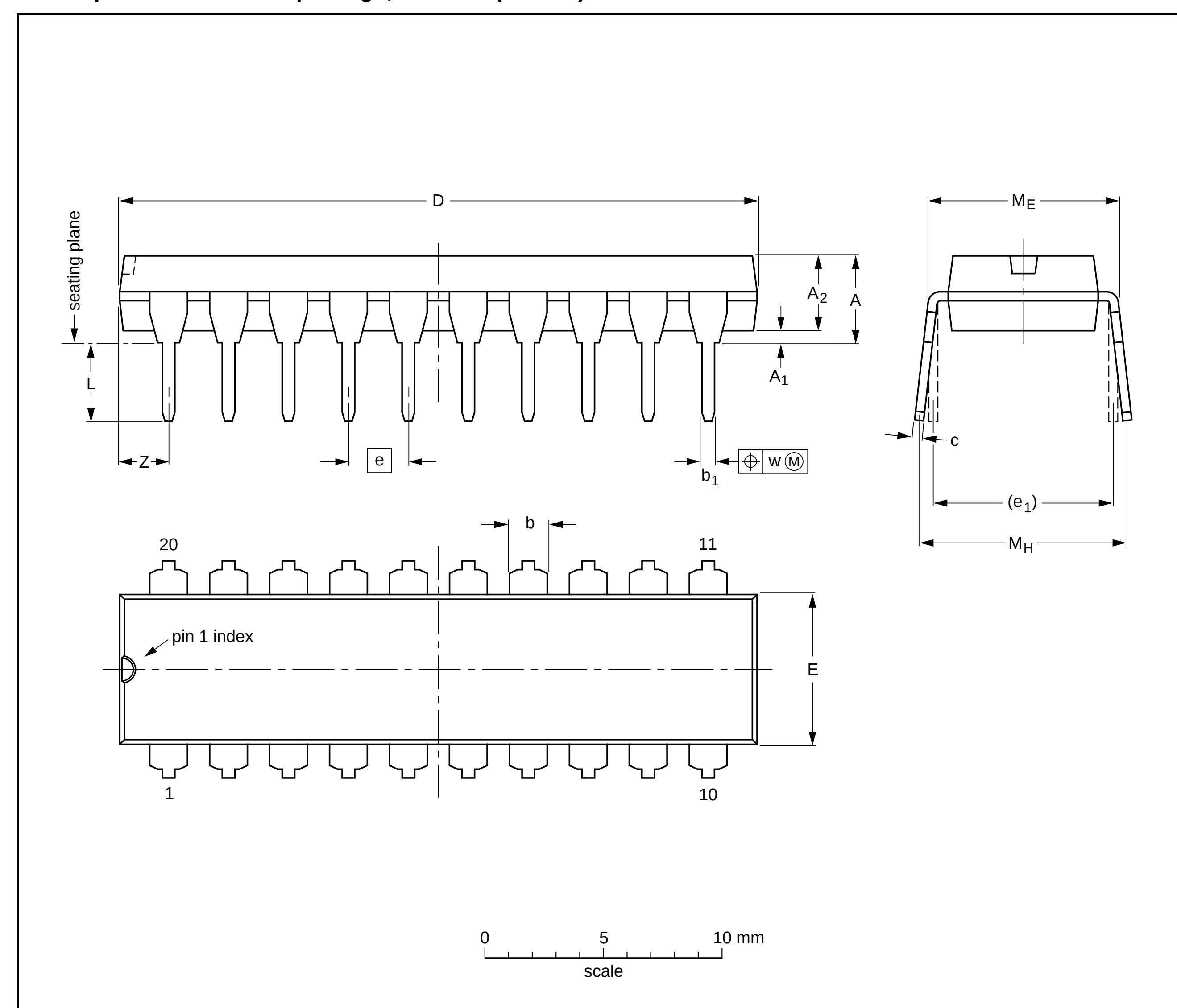


(1) When supplied via a 75 Ω line.

Fig.4 Typical application circuit diagram.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

533061/1100/02/pp12 Date of release: 1996 Jan 09
Document order number: 9397 750 00556

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